5. (Twice amended) The method of claim 1 wherein generating said virtual memory address for said second memory location includes transforming the addresses of said pixel data at said first virtual memory location to addresses at said second memory location.

6. (Amended) The method of claim 5 including determining the offset to pixel data by subtracting a base address at said first virtual memory location from the address of pixel data.

9. (Twice amended) The method of claim 1 wherein writing said transformed pixel data from said first virtual memory location to said second memory location includes writing said pixel data from said first virtual memory location associated with a first transfer function to said second memory location associated with a second transfer function.

11. (Twice Amended) An article comprising a medium storing instructions that enable a processor-based system to:

write pixel data to a first virtual memory location;

perform a first pixel transformation at said first virtual memory location;

generate a virtual memory address for a second memory location;

write said transformed pixel data from said first virtual memory location to the virtual memory address of said second memory location; and

transfer said pixel data to a memory controller using a memory controller client.

12. Cancelled.

13. (Amended) The article of claim 11 further storing instructions that enable the processor-based system to write pixel data to a virtual memory location associated with a memory controller client that receives pixel data written to certain virtual addresses.



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15. (Amended) The article of claim 11 further storing instructions that enable the processor-based system to transform the addresses of pixel data at said first virtual memory location to addresses at said second memory location.

16. (Amended) The article of claim 15 further storing instructions that enable the processor-based system to determine the offset to each pixel data by subtracting a base address at said first virtual memory location from the address of each pixel data.

19. (Twice amended) The article of claim 11 further storing instructions that enable the processor-based system to write said pixel data from said first virtual memory location associated with a first transfer function to said second memory location associated with a second transfer function.

21. (Amended) A system comprising:

a memory controller that receives pixel data and virtual memory addresses;

a first memory controller client that forwards the pixel data and virtual memory addresses to a first transfer function; and

a second memory controller client that receives data from said first transfer function together with new virtual memory addresses.

22. (Twice amended) The system of claim 21 wherein said first memory controller client selectively forwards the pixel data and virtual memory addresses to one of a plurality of transfer functions and said second memory controller client receives the pixel data with new virtual memory addresses from said plurality of transfer functions.

23. (Amended) The system of claim 22 wherein said second memory controller client writes the pixel data back to said memory controller.



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